

5 laser annealing the amorphous semiconductor material to form a  
6 single crystalline semiconductor layer containing germanium;  
7 doping the single crystalline semiconductor layer and the substrate  
8 at a source location and a drain location to form a source region and a drain  
9 region, whereby a channel region between the source region and the drain  
10 region includes a thin semiconductor germanium region; and  
11 siliciding the source region and the drain region to form a silicide  
12 layer, the silicide layer extending into the substrate.

11. (Thrice Amended) The method of claim 1, further comprising:

2 providing a second amorphous semiconductor material above the  
3 amorphous semiconductor material including germanium after the laser  
4 annealing step;

5 performing another laser annealing step to form a second single  
6 crystalline semiconductive layer from the second amorphous semiconductor  
7 material; and

8 wherein the siliciding step forms the silicide layer so that the  
9 depth of the silicided layer is deeper than the second single crystalline  
10 semiconductor layer.

12. (Twice Amended) A method of manufacturing an ultra-large scale  
12 integrated circuit including a transistor, the method comprising steps of:

13 depositing an amorphous silicon germanium material above a top  
14 surface of a semiconductor substrate;

15 first annealing the amorphous silicon germanium material;

16 depositing an amorphous silicon material above the silicon  
17 germanium material;

18 second annealing the amorphous silicon material; and

19 providing a source region and a drain region for the transistor, the  
20 source region and the drain region being deeper than a combined thickness of  
21 the silicon germanium material and the silicon material.

Please add new Claim 29

29. (New) The method of claim 12 further comprising:

*2*  
*Concluded*

siliciding the source and the drain region to form a silicide layer, wherein the silicide layer extends deeper than the combined thickness.

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